"Invited"-Picosecond Imaging Circuit Analysis of ULSI Microprocessors

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ABSTRACT — **Picosecond Imaging Circuit Analysis (PICA) is a high speed backside emission based tool used for timing analysis of ULSI circuits. It was invented at IBM in 1996, and has been used since then to help deliver microprocessors profitably. As a fault localization tool, PICA has been used to find and diagnose stuck at faults, races, shorts, and leaking devices as well as many other failure mechanisms. The combination of timing resolution on the order of 20 ps, and sub micron spatial resolution enables the probing of many individual transistors in parallel in complex high speed circuit designs. The timing analysis from PICA can also be used to debug and improve designs while running chips at speed by measuring the timing at which transistors switch, and comparing the results to simulated values. Here we will describe the technique as well as demonstrate its use during the debug of an I/O circuit defect found on the IBM System/390 G5 microprocessor.**

I. PICOSECOND IMAGING CIRCUIT ANALYSIS

PICA (Picosecond Imaging Circuit Analysis[1-5]) was invented at IBM to enable diagnostics of flip-chip mounted ULSI chips. It is a non-invasive backside tool used to measure the timing of switching events on CMOS circuits running at speed. Gate level performance can then be compared to models in order to identify the nature of a fault. In this paper we will describe how PICA works and demonstrate its use in diagnosing a faulty I/O on the IBM System/390 microprocessor.

Infrared light is emitted from the channel of a CMOS transistor whenever current flows, as is shown in Figure 1. The source of the light is hot electron emission in the pinch off region of the device. The photons escape through the substrate of the device under test (DUT) and are captured by an infrared detector, which records their time of arrival, as well as the position on the chip that they originated from, shown in Figure 2. The resulting images show the integration of all the photons emitted as a function of time when the device switched, for all the devices in the field of view of the detector. One can then localize a defect visually (by observation if one device appears to perform differently than others in the field of view) or by extracting the optical waveform (number of photons as a function of time) for a particular device and comparing to either a known good device, or to models. An accurate localization of a defect dramatically increases the likelihood of properly diagnosing a failure's root cause as well as saving valuable time.

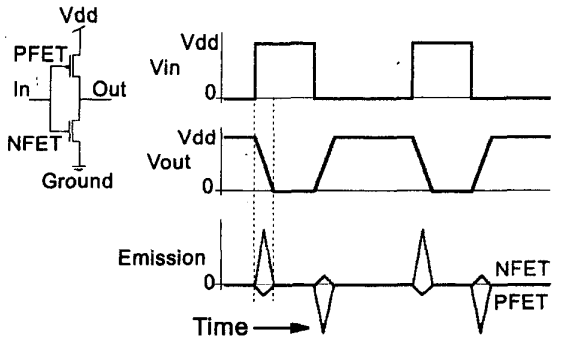

Figure 1 Simulated emission from the switching activities of FETs in CMOS.

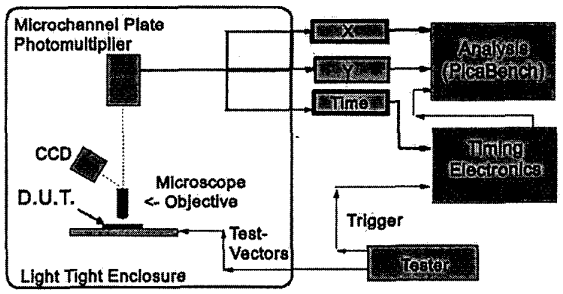

Figure 2 Basic layout of a PICA tool showing the microscope used for navigation, the infrared detector, tester clock and timing electronics.

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II. PICA METHODOLOGY

The microprocessor to be analyzed is first thinned to less than 100μm in order to minimize losses due absorption in the silicon The part is then flip-chip mounted in a test board under the microscope of the PICA tool. The choice of the region to measure is often predetermined by tester diagnostics. Regions varying from 180 μm^2 up to 12 mm^2 are generally available, allowing for the analysis of some 10k devices up to full chip views. The part is stimulated using a tester running a test loop, causing the fail to occur in a repeatable fashion. The timing electronics are triggered by the tester's clock. The whole apparatus is enclosed in a light tight box, and mounted on an air table to minimize vibrations, as is shown in Figure 2. A commercially available tool, the IDS-PICA, is available from Schlumberger Semiconductor Solutions[i].

PICA is a statistical method, therefore the longer you acquire data, the better the signal to noise ratio. Aside from thinning the substrate to capture as many of the emitted photons as possible, it also proves useful to exercise the part in short test loops in order to minimize the acquisition length. A judicious choice of a short loop length pattern that causes the circuits under examination to cycle quickly through the desired switching states also accelerates the measurement greatly.

II. CASE STUDY: FAULTY I/O CIRCUIT

The case study demonstrates the use of PICA in the identification of an I/O circuit defect found on the IBM System/390 G5 microprocessor, which is built in 0.25 μm technology and designed to run at 500Mhz.

Multi-chip module testing showed an unusually high number of timing failures on chip-to-chip paths as a known good chip changed from receive mode to drive mode while the bad chip went from drive to receive mode. The bad chip took tens of nanoseconds to achieve the right state: the source of the problem was suspected to be a random defect on the I/O circuit, causing the timing problem. A schematic of the I/O circuit under the failing condition is shown in Figure 3. Here, Y is slow to transition from 1 to 0 as the disable (DI) is switched from 1 to 0 and A is held at 0. The electrical test pinpointed transistor T25, gates 1 and 3 and a possible wire short or open as possible sources of the timing behavior. The potentially prohibitive time expected in performing failure analysis of all the possible causes indicated that PICA ought be performed in order to further localize the fail. The I/O circuit can be enabled/disabled by toggling the signal DI through a test I/O.

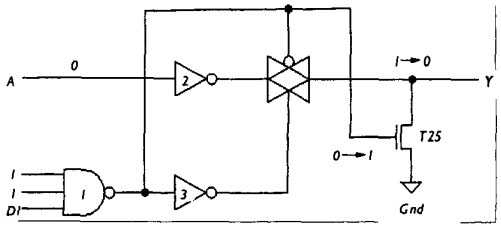

Figure 3 Simplified schematic of the I/O circuit showing transistor T25.

PICA was performed over an area containing several I/Os and gave the time integrated image shown in Figure 4, where the emission coming from T25 is circled for a defective I/O in the upper part, and for a good I/O in the lower portion. The waveforms shown below each emission image are the optical waveform extracted from the circled area, and therefore represent the timing from a defective I/O, and a good I/O respectively.

A. PICA Timing Analysis

A full layout to schematic mapping allows one to extract the optical waveforms from the individual devices of which the I/O is built. The predicted switching activity of a device can then be compared to the measured activity.

The extracted waveforms show the nature of the timing fault quite clearly: the detective I/O doesn't switch as quickly as the good one, taking roughly 12 ns more to do so. Further analysis of the optical waveforms led to the discovery that the waveforms from gate 1 and gate 3 were similar for both good and defective I/Os, and matched simulated emission from these gates. This led to the conclusion that the defect was localized either on T25 or on the wires connecting T25 to gate 1.

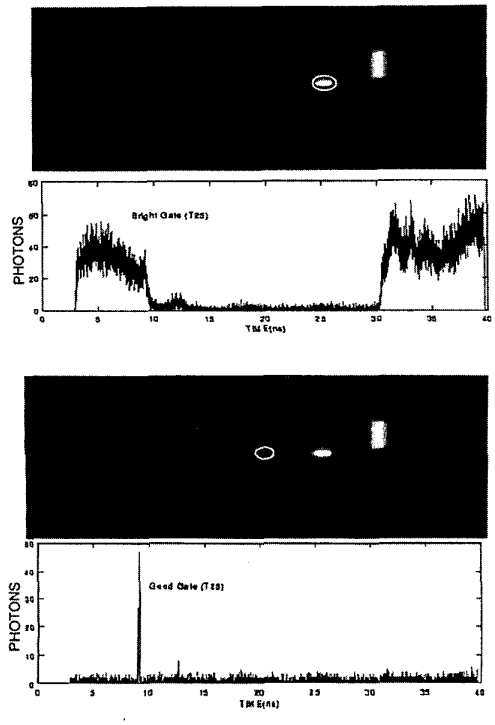

Figure 4 Integrated emission measurements of defective I/O, upper figure, and good I/O, lower figure, showing the areas associated with T25 circled in white. The optical waveforms associated with T25 of each I/O are shown.

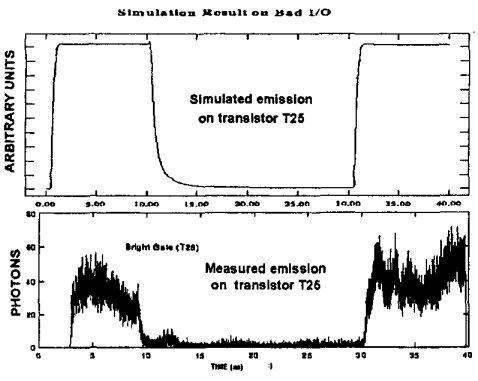

Figure 5 Simulated optical waveform from T25 is compared to measured waveform from bad I/O.

B. Circuit Simulation

In order to fully localize the defect, circuit simulations were used. All possible defects were injected into the simulator, and the resulting modeled emissions were then compared with the measured optical waveforms. The results show that the emission caused by a highly resistive wire matches that of the defective I/O: the top part of Figure 5 shows the simulated waveform of the source to drain current of T25 with a resistance on its gate, the bottom part the measured emission from the faulty T25. With the fault localized to T25's gate, the part was sent to physical failure analysis where a highly resistive wire-to-wire contact was found. The results of failure analysis are shown in Figure 6, which also shows the schematic of the fault used for modeling the emission.

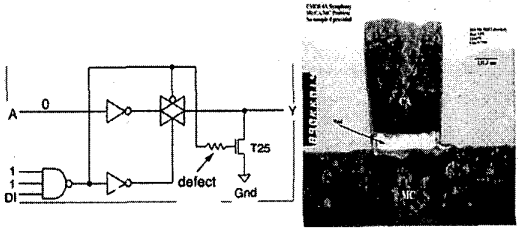

Figure 6 Schematic of defective I/O used for modeling and TEM image of the defect showing a highly resistive wire-to-wire contact.

III. Conclusions

The case study described here demonstrates one use of PICA: fault localization. The precision with which a defect can be pinpointed leads to huge savings in avoided failure analysis costs, as well as speeding redesign efforts if they are called for. The parallel nature of PICA was used here to examine the behavior of several I/Os simultaneously thus leading to faster diagnosis.

At IBM we have also used PICA to measure skew on ULSI microprocessors, tighten timing

on dynamic logic circuitry, measure the effects of degradation, as well as characterize the performance of many test circuits. All these activities are aimed at improving designs and delivering more robust processors.

PICA has the ability to measure timing with an accuracy of tens of picoseconds on individual transistors, large macros, and circuits up to full chip analysis.

Efforts aimed at extending its use to mixed-signal circuits are underway.

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[i] A commercially available tool, the IDS®-PICA, is available from Schlumberger Semiconductor Solutions. IDS is a registered trademark of Schlumberger.